





INTEGRATED SYSTEMS AND CIRCUITS DESIGN

MASTER | WORK-FRIENDLY


 **Location:** Campus Villach
Europastraße 4, 9524 Villach


 **Duration:** 4 semesters

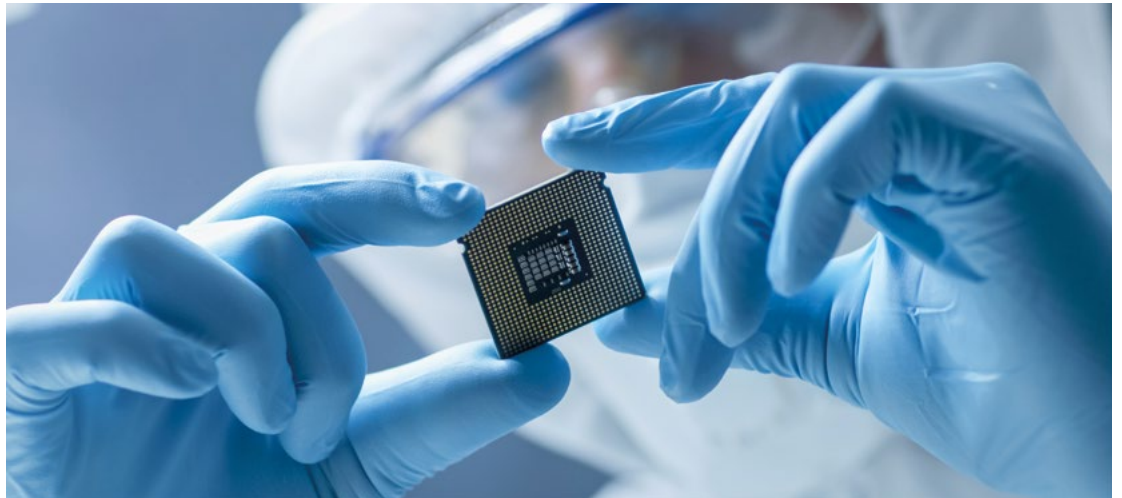
 **Schedule:**
Mon.-Fri. starting at 4:00 pm,
Sat. occasional, work-friendly-schedule

 **Academic Degree:**
Master of Science in Engineering (MSc)

 **ECTS Credits:** 120

 **Language:** English

 **Study places per year:** 20



Integrated circuits have seen an unprecedented development over the last six decades. Fabrication technologies with structure sizes down to 14 nm allow always more complex, more reliable and more cost efficient solutions, reaching new application areas. Due to new requirements and especially due to the enormous complexity, new challenges in the design of integrated systems and circuits have to be faced. The master degree programme ISCD – Integrated Systems and Circuits Design provides the necessary knowledge to master these challenges.

COURSE INFORMATION

The curriculum offers 2 semesters of mandatory courses and allows specialization in the more analogue or digitally dominated domain through elective courses in semester 3 and a thesis work which is accompanied by seminars with presentations and technical discussions in semester 4.

The practical aspect of this master degree programme is emphasized by a project module, spanning semester 1 to 3. With first preparations during semester 1, students design an integrated circuit in small teams and implement a testchip during semester 2. After fabrication of the testchip, samples will be available in semester 3 for evaluation in the lab using state of the art test equipment.

JOBS AND CAREER

The typical graduate will be working for integrated circuit manufacturers, fabless foundries, design houses or suppliers of system solutions using VLSI components. Target employers will be Austrian and international companies.

Research and development in the field of microelectronics is done in close cooperation with Austrian and international partners. It offers students the possibility to participate in the form of master thesis or internships. For more information on current and completed projects in the area of microelectronics:

www.fh-kaernten.at/iscd

CURRICULUM

1 st Semester	SCH	ECTS
Design of Digital Integrated Circuits	4	6
Integrated Circuits Technology	2	3
Introduction to Computer Aided Design	4	6
Design of Analog Integrated Circuits	5	7,5
Introduction to Project	2	3
Basics in Systems and Circuits Theory	2	2,5
Foreign Language (1)	2	2
Total	21	30

2 nd Semester	SCH	ECTS
Advanced Topics in Analog Integrated Circuits	5	7,5
Computer Aided Design	2	3
System Modeling and Verification – Digital	3	4,5
Digital Design with HDL	5	7,5
IC Design and Implementation	4	5,5
Foreign Language (2)	2	2
Total	21	30

3 rd Semester	SCH	ECTS
Testing of Integrated Circuits	3,5	4,5
System Modeling and Verification – Analog	2	3
IC Evaluation	1,5	2,5
Elective Courses 1	7	10
Analog and Mixed-Signal ICs for Communication Systems	3,5	5
Integrated Data Converters	3,5	5
System-on-Chip Architectures	3,5	5
Special Topics in VLSI/SoC/SiP Design – 1	3,5	5
Elective Courses 2	7	10
Advanced Topics in Digital Integrated Circuits	3,5	5
Integrated Sensors for Automotive Applications	3,5	5
Arithmetic Modules for VLSI/SoC Design	3,5	5
Special Topics in VLSI/SoC/SiP Design – 2	3,5	5
Total	21	30

4 th Semester	SCH	ECTS
Master Thesis	16	24
Master Thesis Seminar	4	6
Total	20	30
Total Sum	83	120

SCH = Semester Credit Hour

ECTS = European Credit Transfer System



What I appreciated most were the modern labs, the software and the state-of-the-art equipment. The lectures were taught in English and the students came from different nations. Studying ISCD offered me the possibility to take part in research projects as well.

GRACIELE BATISTELL, MSc
ISCD graduate

📅 DATES

Start: October 2022

Study Info Lounge: always on the second Tuesday of the month from 2 p.m. to 6 p.m. - ONLINE

FH Days and information events:

all dates at www.fh-kaernten.at/fhday

💶 COSTS

Tuition fee: € 363,36 per semester

Student Union Fee: around € 20, annual adjustment

✉ CONTACT

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